



N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

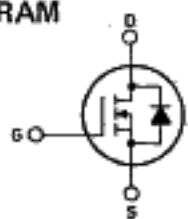
V_{DSS}	$R_{DS(ON)}$	I_D
180V/200V	0.4 Ω	8 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP	
		8N18	8N20
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	180V	200V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	180V	200V
V_{GS}	Gate-source voltage	$\pm 20V$	
I_D	Drain current (continuous) $T_{case} = 25^\circ C$	8A	
$I_{DM}^{(*)}$	Drain current (pulsed)	25A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at $T_{case} = 25^\circ C$	75W	
	Derating factor	0.6W/ $^\circ C$	
T_{stg}	Storage temperature	-65 to 150 $^\circ C$	
T_j	Max. operating junction temperature	150 $^\circ C$	

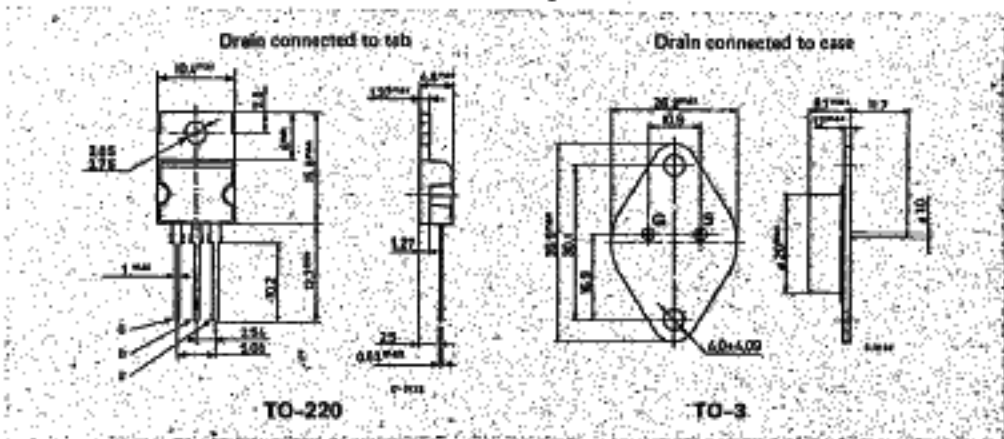
(*) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

$R_{th(j-case)}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{DS(oss)}$	Drain-source breakdown voltage	$I_D = 5\text{ mA}$ $V_{GS} = 0$ for SEFM8N18/SEFP8N18 for SEFM8N20/SEFP8N20	180 200			V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 0.85 \text{ Rated } V_{DSS}$ $T_J = 100^\circ\text{C}$			250 2.5	μA mA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			500	nA

ON*

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$ $T_J = 100^\circ\text{C}$	2 1.5		4.5 4.0	V V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ $I_D = 4\text{ A}$		0.27	0.4	Ω
$V_{DS(on)}$	Drain-source On voltage	$V_{GS} = 10\text{ V}$ $I_D = 8\text{ A}$ $V_{GS} = 10\text{ V}$ $I_D = 4\text{ A}$ $T_J = 100^\circ\text{C}$			4 3.2	V V
g_{fs}	Forward transconductance	$V_{DS} = 15\text{ V}$ $I_D = 4\text{ A}$	3			mho

DYNAMIC

C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		980	1200	pF
C_{oss}	Output capacitance			200	260	pF
C_{rss}	Reverse transfer capacitance			80	100	pF



SEFMN820
SEFP8N18
SEFP8N20

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit.
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SWITCHING

$t_{d(on)}$	Turn-on delay time	$V_{CC} = 25\text{ V}$ $I_D = 0.5 \text{ Rated } I_D$ $R_{GS} = 50\ \Omega$ $R_L = 50\ \Omega$ (see test circuit)	40		ns
t_r	Rise time		150		ns
$t_{d(off)}$	Turn-off delay time		100		ns
t_f	Fall time		100		ns

SOURCE DRAIN DIODE

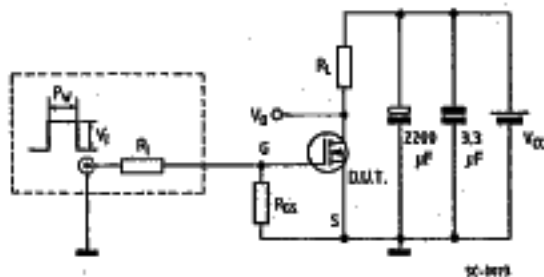
V_{SD}	Forward on voltage	$I_{SD} = \text{Rated } I_D$ $V_{GS} = 0$	2.0		V
t_{on}	Forward Turn-on time		250		ns
t_r	Reverse recovery time		325		ns

* Pulsed: pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

For typical curves, and clamping inductive load, gate charge, body drain diode tr measurement test circuits see SGSP363 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width $\leq 100\ \mu\text{s}$
Duty cycle $\leq 2\%$
 $V_G = 10\text{ V}$

Waveforms

